AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method for processing variable width instructions in a pipelined processor, comprising:

decoding instructions to identify a loop setup instruction having a loop setup instruction address ~~and containing~~ to determine a loop top offset indicative of a loop top instruction address of a loop top instruction and a loop bottom offset indicative of a loop bottom instruction address of a loop bottom instruction;

decoding a current instruction ~~instructions~~ following the loop setup instruction, the current instruction ~~each~~ having ~~an~~ a current instruction address and ~~containing an~~ a current instruction width; ~~and~~

~~for each instruction following the loop setup instruction, using a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset to determine~~ determining if [[the]] a next instruction to be decoded is ~~a~~ the loop bottom instruction based, at least in part, on the current instruction address, the current instruction width, the loop setup instruction address and the loop bottom offset;

providing the loop top instruction address to an instruction fetch stage of the pipelined processor if it is determined that the next instruction is the loop bottom instruction, and

fetching the loop top instruction prior to completing a decoding of the loop bottom instruction.

2. (Original) A method as defined in claim 1, wherein determining if the next instruction is a loop bottom instruction comprises determining if the current instruction address plus the current instruction width minus the loop setup instruction address minus the loop bottom offset is equal to zero.

3. (Currently amended) A method for processing variable width instructions in a pipelined processor, comprising:

decoding instructions to identify a loop setup instruction having a loop setup instruction address and containing a loop bottom offset;

decoding instructions following the loop setup instruction, each having an instruction address and containing an instruction width; [[and]]

for each instruction following the loop setup instruction, using a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset to determine if the next instruction is a loop bottom instruction, wherein determining if the next instruction is a loop bottom instruction comprises determining if the current instruction address plus the current instruction width plus the loop setup instruction address inverted plus the loop bottom offset inverted plus 1 is equal to negative 1; and

changing a state of a loop bottom register if it is determined that the next instruction is the loop bottom instruction to indicate to the pipelined processor that a loop top instruction should be fetched.

4. (Original) A method as defined in claim 3, wherein the step of determining if the next instruction is a loop bottom instruction is performed by a plurality of adders, a plurality of exclusive OR gates receiving outputs of the adders and an AND gate receiving outputs of the exclusive OR gates.

5. (Original) A method as defined in claim 1, further comprising identifying a next instruction following the loop setup instruction as a loop bottom instruction if the loop bottom offset is equal to a width of the loop setup instruction.

6. (Currently amended) Apparatus for processing variable width instructions in a pipeline processor, comprising:

an instruction decoder configured to decode a loop setup instruction, having a loop setup instruction address, to obtain a loop top offset indicative of a loop top instruction address of a loop top instruction and a loop bottom offset indicative of a loop bottom instruction address of a loop

bottom instruction and configured to decode instructions following the loop setup instruction, each having an instruction address, to obtain an instruction width;

an instruction fetch stage configured to fetch instructions to be decoded by the instruction decoder;

registers for holding the loop setup instruction address and the loop bottom offset, respectively; and

a loop bottom detector~~, responsive to a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset,~~ configured to determine if a next instruction to be decoded is [[a]] the loop bottom instruction based, at least in part, on a current instruction address and current instruction width of a current instruction being decoded by the instruction decoder, and configured to provide the loop top instruction to the instruction fetch stage prior to completing a decoding of the loop bottom instruction if the loop bottom detector determines the next instruction is the loop bottom instruction.

7. (Currently amended) Apparatus for processing variable width instructions in a pipeline processor, comprising:

an instruction decoder configured to decode a loop setup instruction, having a loop setup instruction address, to obtain a loop bottom offset and configured to decode instructions following the loop setup instruction, each having an instruction address, to obtain an instruction width;

registers for holding the loop setup instruction address and the loop bottom offset;

a loop bottom register for holding a state indicative of whether a loop bottom instruction has been detected; and

a loop bottom detector, responsive to a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset, configured to determine if a next instruction is a loop bottom instruction, wherein the loop bottom detector is configured to determine if the current instruction address plus the current instruction width plus the loop setup instruction address inverted plus the loop bottom offset inverted plus one is equal to negative one, and wherein the loop bottom detector is configured to change the state of the loop bottom register if it is determined that the next instruction is the loop bottom instruction.

8. (Original) Apparatus as defined in claim 7, wherein the loop bottom detector comprises a plurality of adders receiving the current instruction address, the current instruction width, the loop setup instruction address inverted, the loop bottom offset inverted and one, a plurality of exclusive OR gates receiving outputs of the adders and an AND gate receiving outputs of the exclusive OR gates to provide a loop bottom indication.

9. (Currently amended) Apparatus for processing variable width instructions in a pipelined processor, comprising:

means for decoding a loop setup instruction, having a loop setup instruction address, to obtain a loop top offset indicative of a loop top instruction address of a loop top instruction and a loop bottom offset indicative of a loop bottom instruction address of a loop bottom instruction and for decoding instructions following the loop setup instruction, each having an instruction address, to obtain an instruction width;

means for fetching instructions to be decoded by the means for decoding;

means for holding the loop setup instruction address and the loop bottom offset; and

means~~, responsive to a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset,~~ for determining if a next instruction to be decoded is [[a]] the loop bottom instruction based, at least in part, on a current instruction address and current instruction width of a current instruction being decoded by the instruction decoder, and configured to provide the loop top instruction to the means for fetching instructions prior to completing a decoding of the loop bottom instruction if the next instruction is determined to be the loop bottom instruction.

10. (Original) Apparatus as defined in claim 9, wherein the means for determining if a next instruction is a loop bottom instruction comprises means for determining if the current instruction address plus the current instruction width minus the loop setup instruction address minus the loop bottom offset is equal to zero.

11. (Currently amended) Apparatus for processing variable width instructions in a pipelined processor, comprising:

means for decoding a loop setup instruction, having a loop setup instruction address, to obtain a loop bottom offset and for decoding instructions following the loop setup instruction, each having an instruction address, to obtain an instruction width;

means for holding the loop setup instruction address and the loop bottom offset; [[and]]

means, responsive to a current instruction address, a current instruction width, the loop setup instruction address and the loop bottom offset, for determining if a next instruction is a loop bottom instruction, wherein the means for determining if a next instruction is a loop bottom instruction comprises means for determining if the current instruction address plus the current instruction width plus the loop setup instruction address inverted plus the loop bottom offset inverted plus one is equal to negative 1; and

means for changing a state of a loop bottom register when it is determined that the next instruction is the loop bottom instruction.

12. (Original) Apparatus as defined in claim 11, wherein the means for determining if the next instruction is a loop bottom instruction comprises a plurality of adders, a plurality of exclusive OR gates receiving outputs of the adders and an AND gate receiving outputs of the exclusive OR gates.